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CATAWBA
AC

405 130

TM 1003 010 00

Milestone 11

160A Computer Program Description

TECHNICAL MEMORANDUM

(TM Series)

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Milestone 11	SYSTEM
160A Computer Program Description	DEVELOPMENT
By	CORPORATION
V. J. Gergen	2500 COLORADO AVE.
26 March 1963	SANTA MONICA
Approved	CALIFORNIA
R. D. Knight	

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26 March 1963

-1-

TM-1003/010/00

PROGRAM IDENTIFICATION

- A. Title: CCC Simulator Program (CCC SIM) - Ident 22C, Mod 00
- B. Programmed: 11 January 1963
 - N. D. Babic, Control Data Corporation
- C. Documented: 26 March 1963
 - N. D. Babic, CDC and V. J. Gergen, SDC

PURPOSE

The CCC Simulator provides a simulated intercommunication link between the Bird Buffer (BB) computer and the Tracking Station (TS) computer that is normally performed by the Computer Communication Converter (CCC) and associated equipment.

USAGE

A. Operating Instructions

- Step 1 Master Clear all three computers before uncabling and recabling.
- Step 2 Use machine load of computer No. 1 to read the paper tape containing the CCC Simulation program into core. Starting location is "0000" Bank "0".
- Step 3 Set Selective Stop Switches 1 and 2 (SLS 1 & SLS 2) on the CCC Simulation computer for error stop indications desired. (See Error Stops below.)
- Step 4 Load interfacing programs into TS & BB computers and put them into the programmed "wait loop" (see Restrictions D, Computer No. 2 = TS, Computer No. 3 = BB).
- Step 5 Set the CCC Simulation computer Program Register (P) = 0000, and set Run/Step switch to "RUN".
- Step 6 Execute a Manual Interrupt on the CCC Simulation computer, e.g., depress a Jump and a Stop key, simultaneously, to start programs into the transmission cycle.

B. Error Stops:

P = 1270 A tracking station computer has failed to take the status code word, if SLS 1 is set.

- P = 1273 A tracking station computer has failed to take the data word, if SLS 2 is set.
- P = 0414 A tracking station computer has attempted to send or receive out of turn.
- P = 1567 A Bird Buffer computer has failed to take a status code word, if SLS 1 is set.
- P = 1572 A Bird Buffer computer has failed to take a data word, if SLS 2 is set.
- P = 0114 A Bird Buffer computer has attempted to send or receive out of turn.

C. I/O Format

1. Inputs

Select Codes - The following select codes can be issued by the BB and TS computers. These select codes will be interpreted by the CCC Simulator program as indicated below:

EFC	ACTION
5500	Transfer a word from the CCC Simulator to the BB (or TS) computer.
5501	Transfer a word from the BB (or TS) computer to the CCC Simulator for relay to TS_1 (or BB_1) computer.
5502	Transfer a word from BB (or TS) computer to the CCC Simulator for relay to TS_2 (or BB_2) computer.
5503	The BB (or TS) requests the present status of the CCC Simulator.
5504 through 5511	No action required of CCC Simulator.

Data Words - The input data word uses the standard 12 bit computer word.

Interrupt 10 - Interrupt 10 is a one time input, when the operator wishes to start the transmission cycles between the computers.

Interrupt 20 - Interrupt 20 is programmed internal to the CCC Simulator. It indicates when the TS computer has an input word for the CCC Simulator on the Internal Buffer channel.

Interrupt 30 - Interrupt 30 is programmed internal to the CCC Simulator. It indicates when the BB computer has an input word for the CCC Simulator on the External Buffer channel.

Interrupt 40 - Interrupt 40 is generated by the CCC adaptor to indicate to the CCC Simulator that the BB computer has requested status from the CCC Simulator. The input is via the CCC Simulator computer's Normal channel.

2. Outputs

CCC Status Words - The CCC Simulation computer outputs a 12 bit status word when requested by the BB or TS computer. The following is the bit interpretation of the Status Code word:

Bit No. (from left to right)	Interpretation
2^0	CCC Simulator has a valid input word for the BB (or TS) computer.
2^2	CCC Simulator is ready to receive a word from the BB (or TS) computer.
2^8	The source of the input word is from the remote number one computer.
2^9	The source of the input word is from the remote number two computer.

The remaining bits are unused and are set to zero.

Interrupt 40 - The Interrupt 40 is generated as a timed output and alternately transmitted to the BB and TS computers.

Data Word - The data word is transferred as the standard 12 bit computer word.

METHOD**A. General**

The CCC simulation program, in a single 160-A computer, assumes the role of two CCC's, the interstation communication equipment, and their associated telephone lines. It provides a method for apparent multiplexing of data as a sending device, and separating and distributing the data to the appropriate computer as a receiving device. It is capable of interfacing with programs, in other 160-A computer, which are programmed such that their 160-A normal channel appears as two computers. The simulation program performs the following functions of the CCC.

1. Within each transmission word time of 13.3 milliseconds, it selects the simulator adaptor to interrupt each apparent computer in the link if a data word directed to that computer is available. The receiving computer is allowed approximately 1.8 milliseconds to service the interrupt and select the word.
2. Within each 13.3 milliseconds interval, it selects the simulator adaptor to interrupt each apparent computer in the link, subject to the priority of 3. whose interrupt is enabled to allow that computer to send a word of data. It maintains a status by means of select codes from the individual computers.
3. It controls the interrupt procedure of 2. such that each apparent 160-A is allowed to send data on a word-by-word priority basis, where the lowest priority is assigned to the computer that sent last.
4. It provides unique sets of status codes to each of the apparent interfacing 160-A computers.

B. Specific

The CCC Simulator program cycles through the following steps.

1. Signal the target computer with an Interrupt 40.
2. Wait for the target computer to issue a request for the CCC Simulator status (EFC 5503). This activates the Interrupt 20 or 30 line. The receipt of this interrupt at this time in the quarter cycle indicates to the CCC Simulator that the target computer has requested status.
3. Reactivate the appropriate output buffer with the status code as a data word.

4. Reactivate the appropriate input buffer for the EFC word, and wait for a 20 or 30 Interrupt. The interrupt at this point in the quarter cycle indicates that the target computer has transmitted the EFC to the CCC Simulator as indicated by the status word to the BB (or TS) computer.
5. Execute the appropriate subroutine.

For EFC 5500:

- a. Reactivate the output buffer with the data word.
- b. Reactivate the input buffer controls.
- c. Wait for an interrupt 20 or 30. Return to 1. if the quarter cycle time runs out. Return to 5. if the interrupt arrives.

For EFC 5501 or 5502:

- a. Reactivate the input buffer and wait for the Interrupt 20 or 30.
- b. After receipt of the interrupt again reactivate the input buffer.
- c. Wait for an interrupt 20 or 30. Return to 1. if the quarter cycle time runs out. Return to 5. if the interrupt arrives.

RESTRICTIONS

- A. The target computer must service the Interrupt 40 in the time allotted (approximately 1.8 milliseconds for the BB and 1.85 milliseconds for the TS). Failure to service the interrupt in time will cause the CCC Simulator program to HALT (See Error Stops, page No. 1).
- B. No other external device can be operated on the normal channel of the TS computer.
- C. The CCC Simulator program is designed to ignore the following EFC's:

<u>EFC</u>	<u>FUNCTION</u>	<u>EFC</u>	<u>FUNCTION</u>
5504	Disable Transmit Interrupt	5508	Not Used
5505	Initiate Resign	5509	Not Used
5506	Enable transmit Interrupt	5510	Enable Test Mode
5507	Not Used	5511	Disable Test Mode

- D. The interfacing TS and HB programs should be programmed with a "Wait" loop as a starting point to allow the CCC Simulator program to start the cycling routine.

E. CPDC System Configuration

The CCC Simulation System is composed of three 160A's: 160A 1 = the CCC Simulator Computer, 160A 2 = the Remote Tracking Station Simulator, and 160A 3 = Bird Buffer Computer; two 169 auxiliary memories: 169 2 is associated with 160A 3, and 169 1 is associated with 160A 1 and the Simulator Adaptor; and various peripheral devices as needed by the HB & TS programs.

The system layout is shown in Figure 1. Note that the Normal Channel of 160A 2 computer is connected to the Internal Buffer Channel of 160A 1, while the 160A 3 computer's Normal Channel is connected to the External Buffer Channel of 160A 1 computer. The Normal Channel of 160A 1 is used, via the CCC Simulator Adaptor, to provide interrupts to 160A's and No. 2 and No. 3.

F. Cabling Instructions for the CPDC Installation

The following cabling connections must be made in order to utilize the CCC Simulator:

1. Remove the cables in the 161 cabinet that jumper to the 1610 and connect to the cables that are marked with black tape, "IN" and "OUT", to the jacks marked "IN" and "OUT", respectively. These are the jacks from which the 1610 cables were removed.
2. Remove the cables from J02 and J04 of 169 1 and connect the cable with the black tag marked J04 to J04.
3. Attach connectors J01 thru J09 to CCC Simulator adaptor in 169 1.
4. Be sure the cables with the black tags marked J02 and J04 in 169 2 are connected to J02 and J04 jacks.
5. A cable diagram is given in Figure 2 which will indicate all other connections that are normal to the CPDC.

TIMING

The CCC Simulation cycle time for the 40 Interrupt is 13.3 milliseconds. Because the 160A computer I/O is not full duplex, this cycle time is broken into four quarter cycles. Each quarter is assigned to an apparent computer (TS₁, TS₂, BB₁, or BB₂). The CCC Simulation Program has a 40 Interrupt schedule where it interleaves the 40 interrupts as follows, TS₁, BB₁, TS₂, BB₂, TS₁, etc. Each of these apparent computers must service the 40 Interrupt within a preset time. It is approximately 1.80 milliseconds for the BB and 1.85 milliseconds for the TS. If no datum is being transmitted between the BB computer and the CCC Simulation computer, the cycle time is 6.7 milliseconds, and 13.3 whenever a datum transfer is required. This is the same for the interface between the CCC Simulator computer and the TS Computer. These 40 interrupts are independent of one another, such that the BB could be on a 6.7 millisecond cycle while the TS is on a 13.3 millisecond cycle time.

STORAGE

Load Start Address	"0000"	Bank 0
END Address	1625 ₈	

VALIDATION TESTS

Two types of validation tests were used, one called the "Test Transmission" program and the second referred to as "BB & TS operational check."

The BB & TS operational check is loaded into both the TS & BB computers. If the cabling and computer Jump switches are set correctly, the CCC Simulator program will cycle with the TS & BB programs, and the three computers will halt at some predetermined point in their respective programs. The P stop number is varied if the cycle time is varied. If the computers fail to cycle, a CDC, CE should be asked to assist in determining the fault. (This program is the second tape in the box that stores the CCC Simulator tape in the CPDC.)

The Test Transmission program (Appendix C) is designed to use the typewriter to print out a "go" condition. If the printout fails and the Jump switches are set correctly, a CDC, CE should be asked to assist in determining the fault. Programs are available with cycle times of 12.1, 13.5 and 13.3 milliseconds or adjust locations 1222 & 1521 as desired.

REFERENCES

SDC Library Document No. 30129, "Report on CCC Simulation", 25 January 1963.

26 March 1963

-8-

TM-1003/010/00

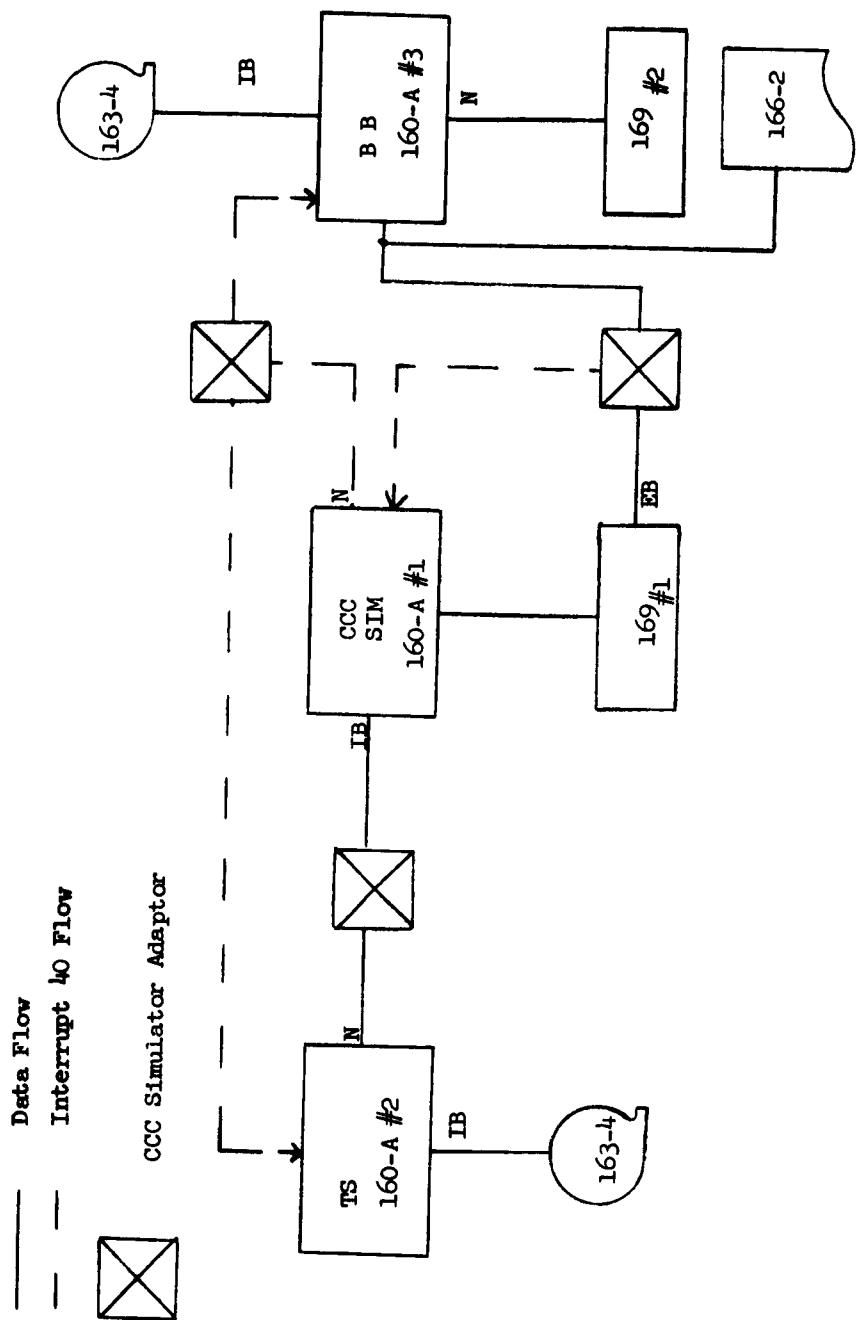


Figure 1: CCC Simulation System

20 March 1963

-9-
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TM-1003/010/00

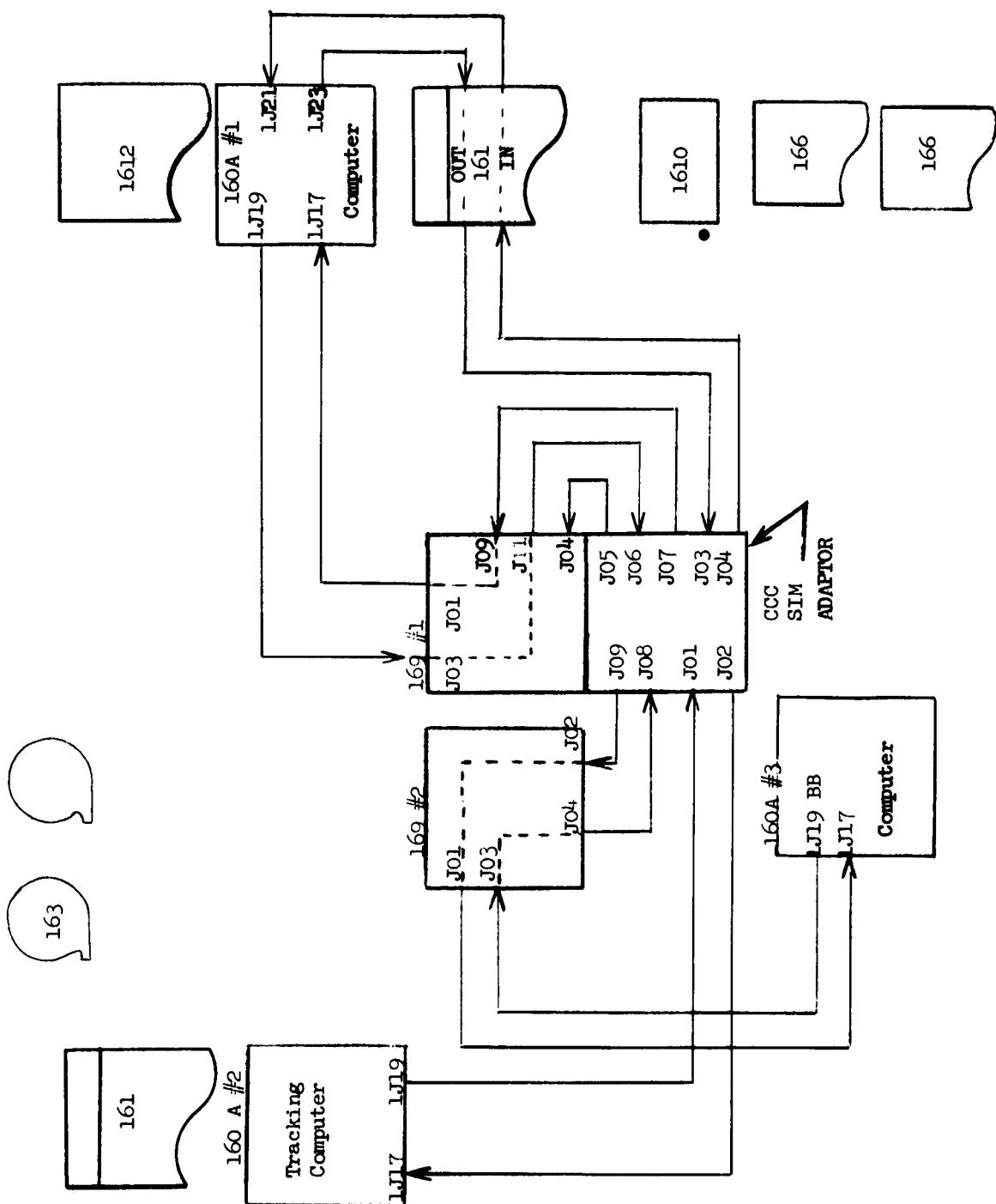
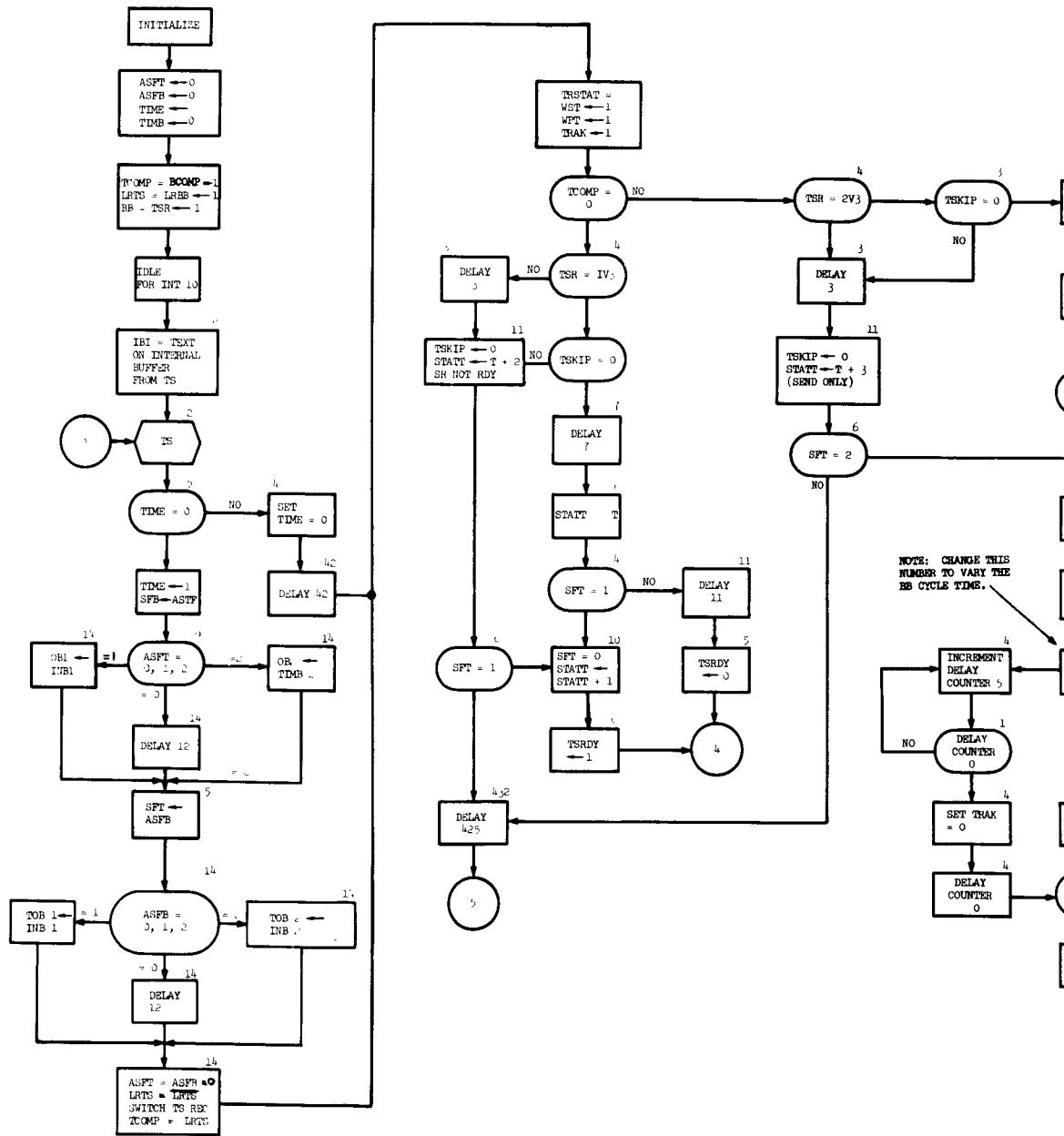


Figure 2: CCC Simulator Cabling

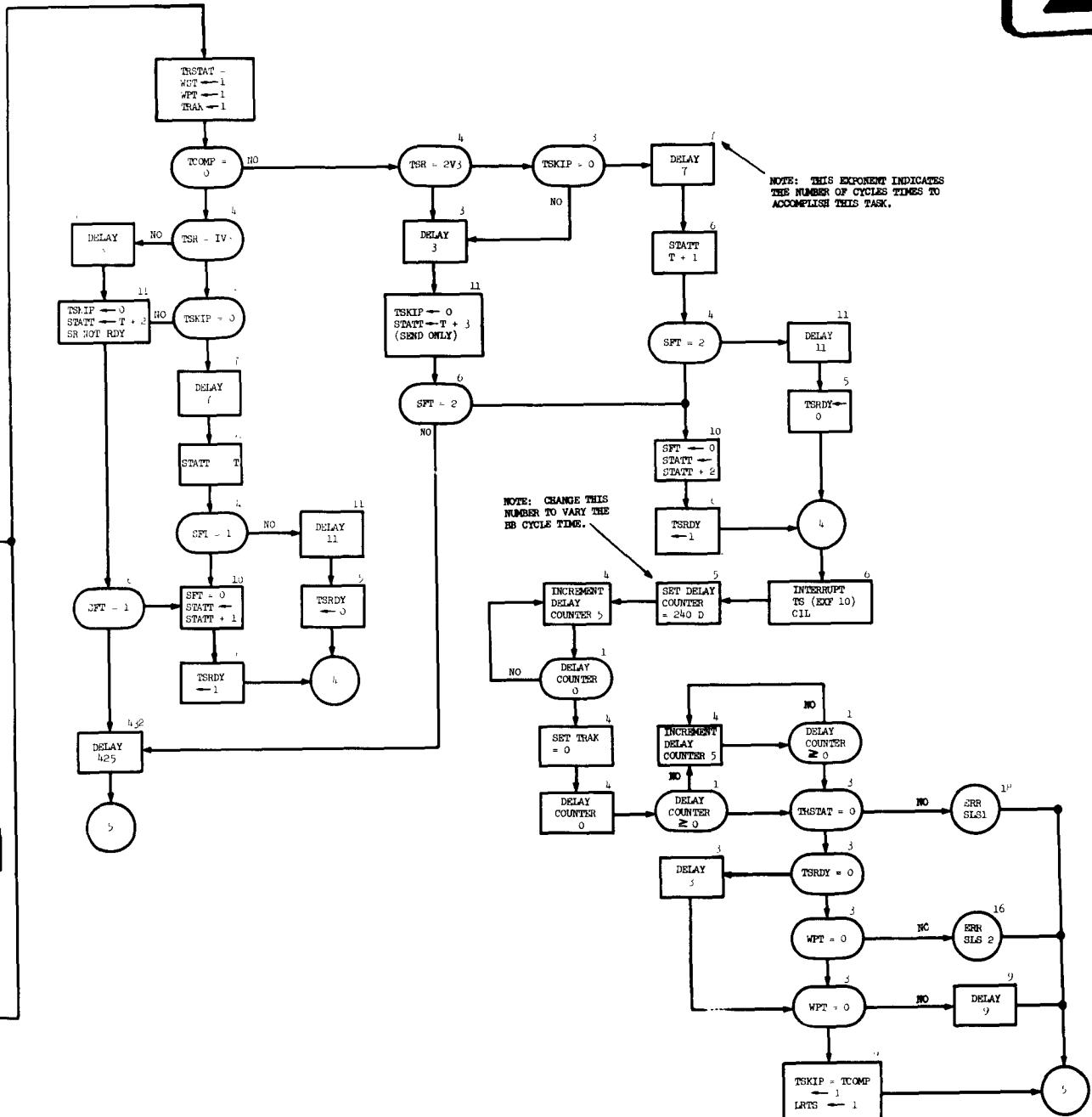
26 March 1963

APPENDIX A



APPENDIX A

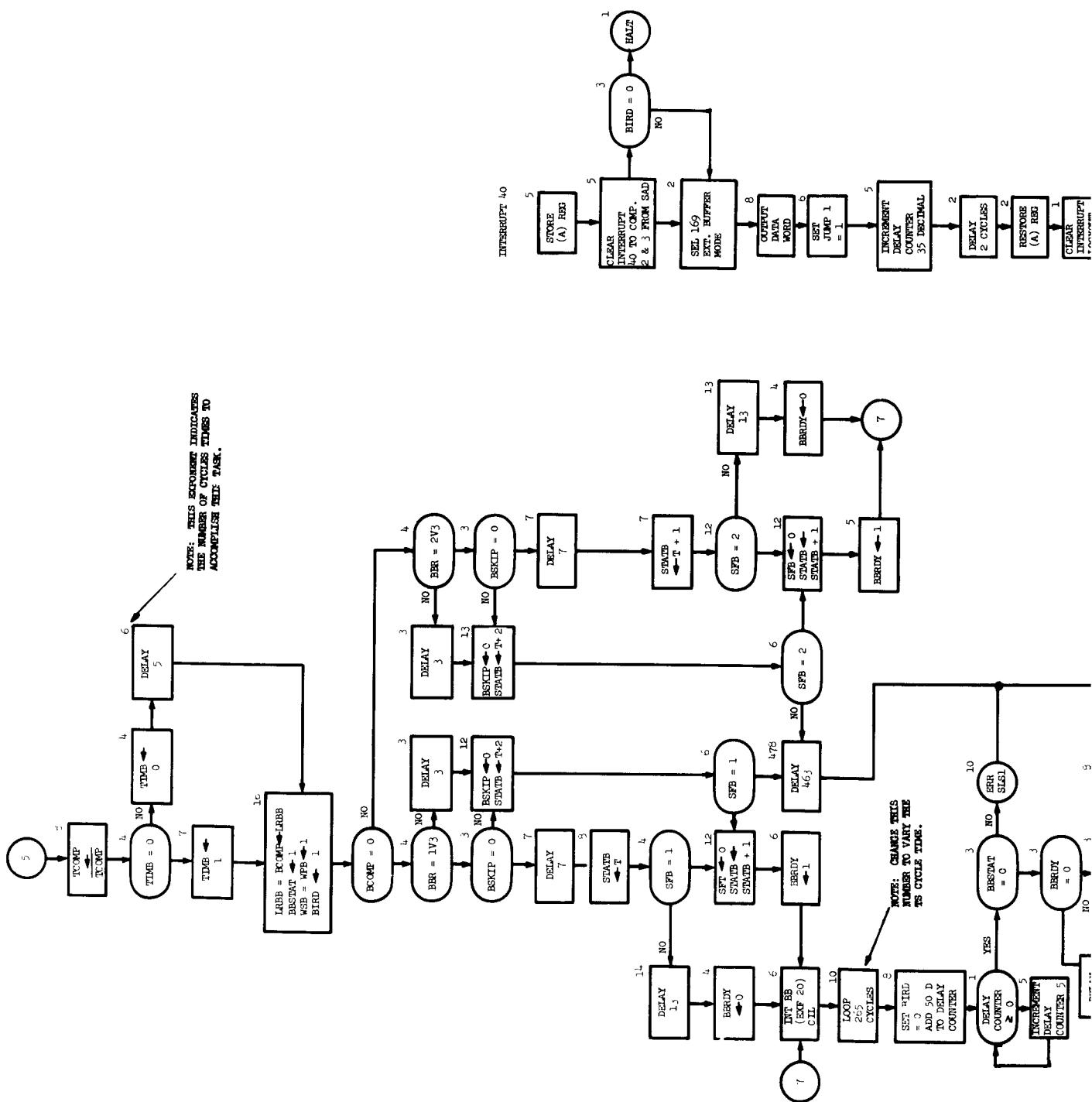
2



26 March 1963

-12-

1



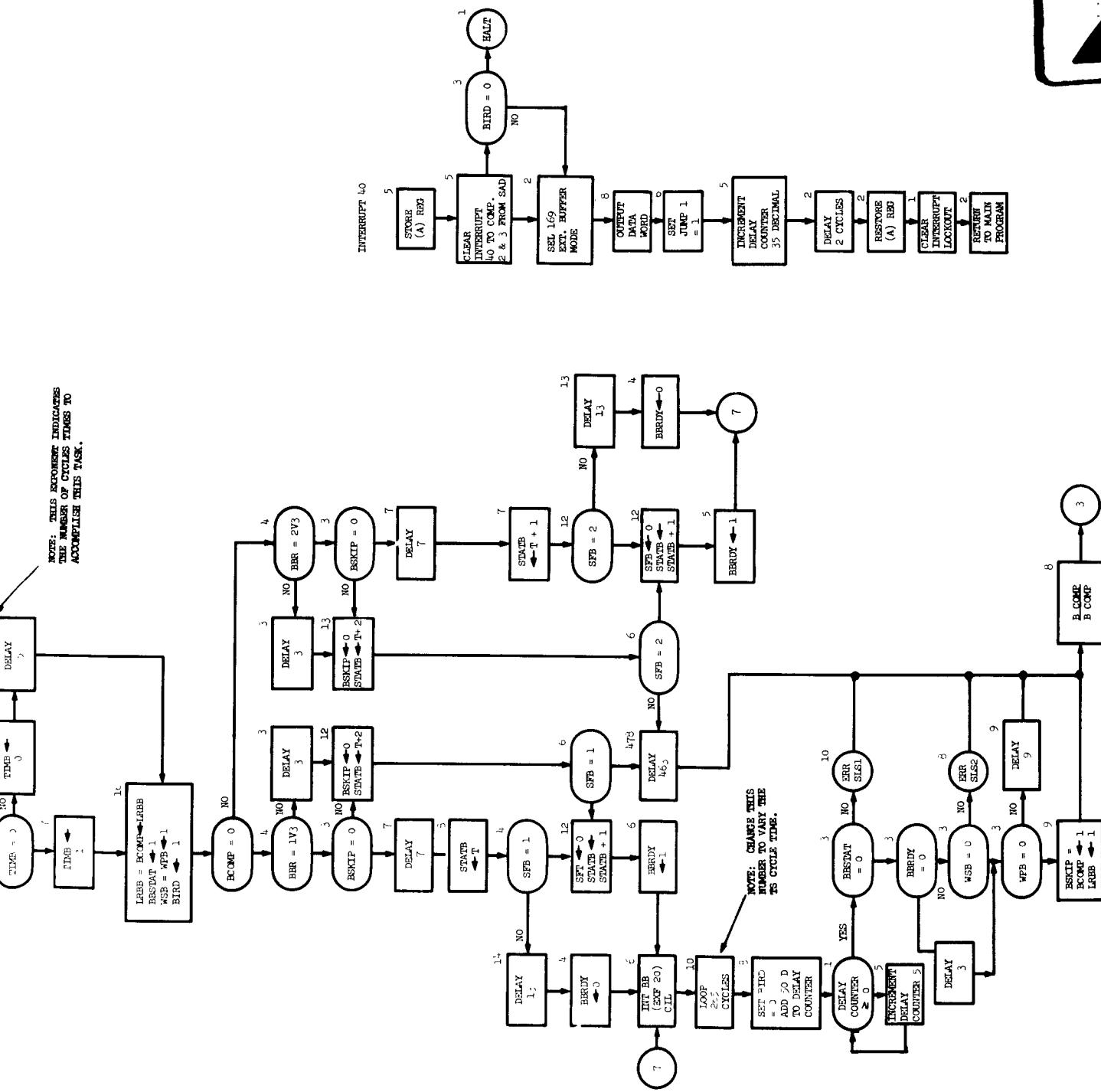
26 March 1963

-12-

TM-1003/010/00

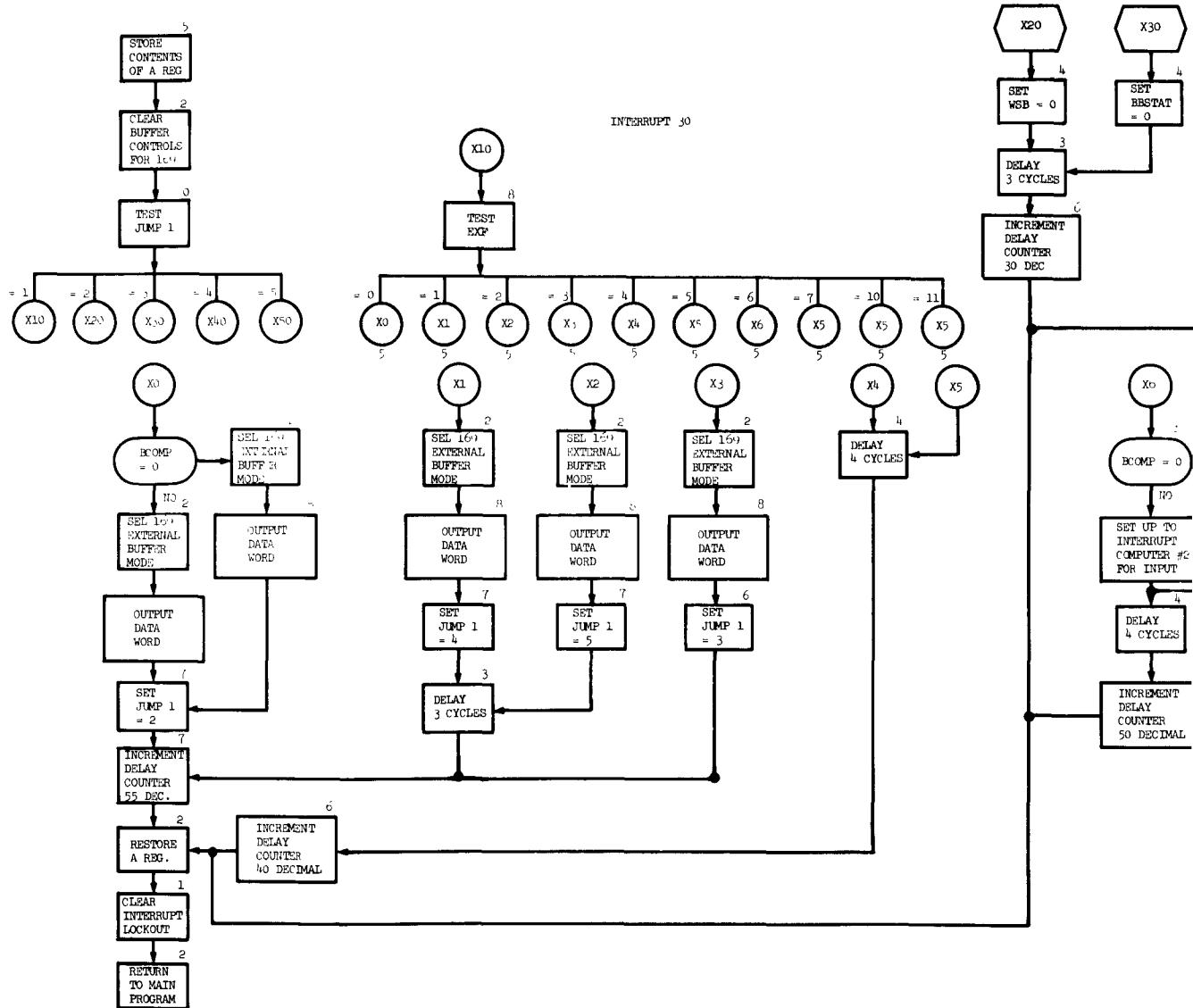
2

NOTE: THIS EXPONENT INDICATES THE NUMBER OF CYCLES TIMES TO ACCOMPLISH THIS TASK.



26 March 1963

-13-

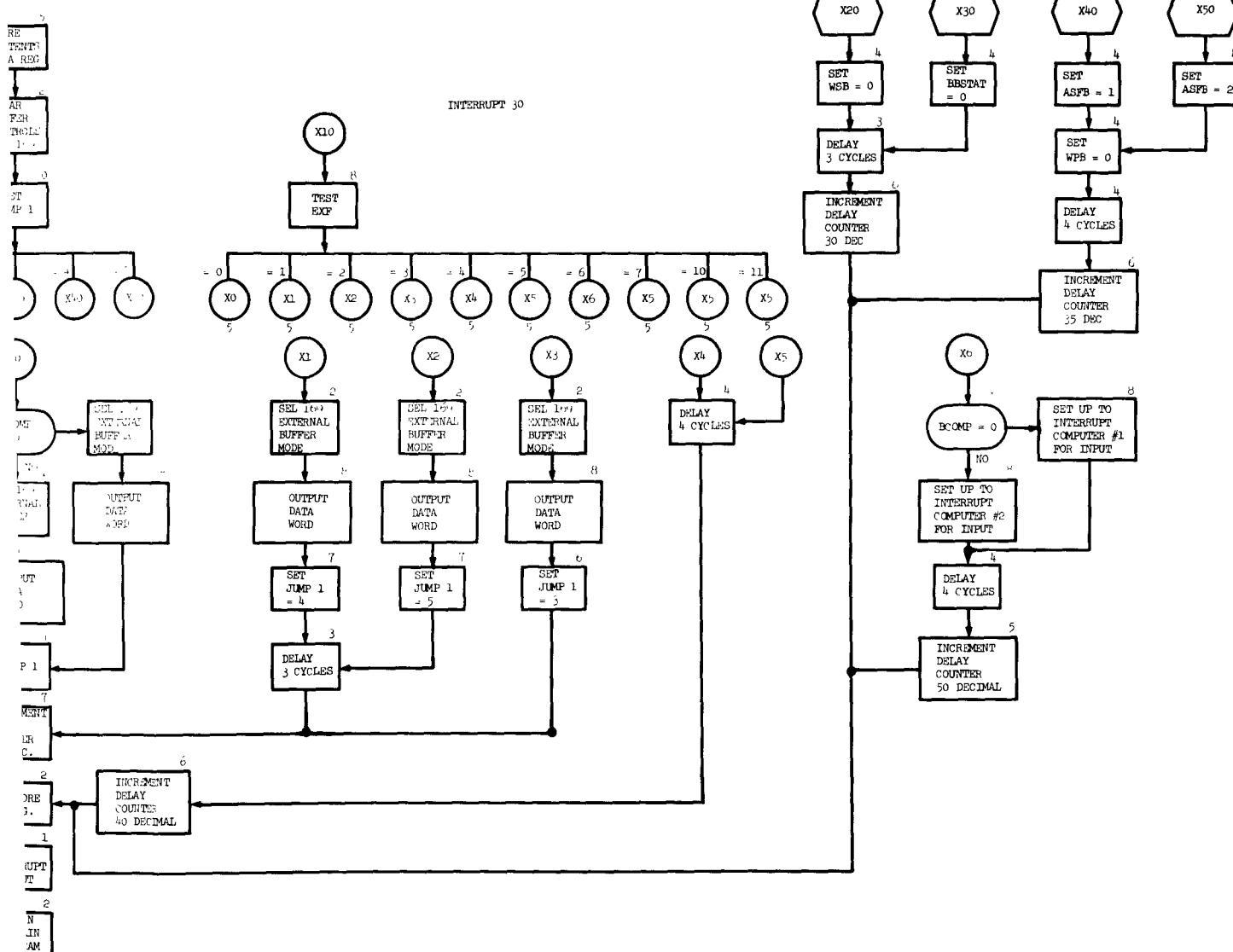


26 March 1963

-13-

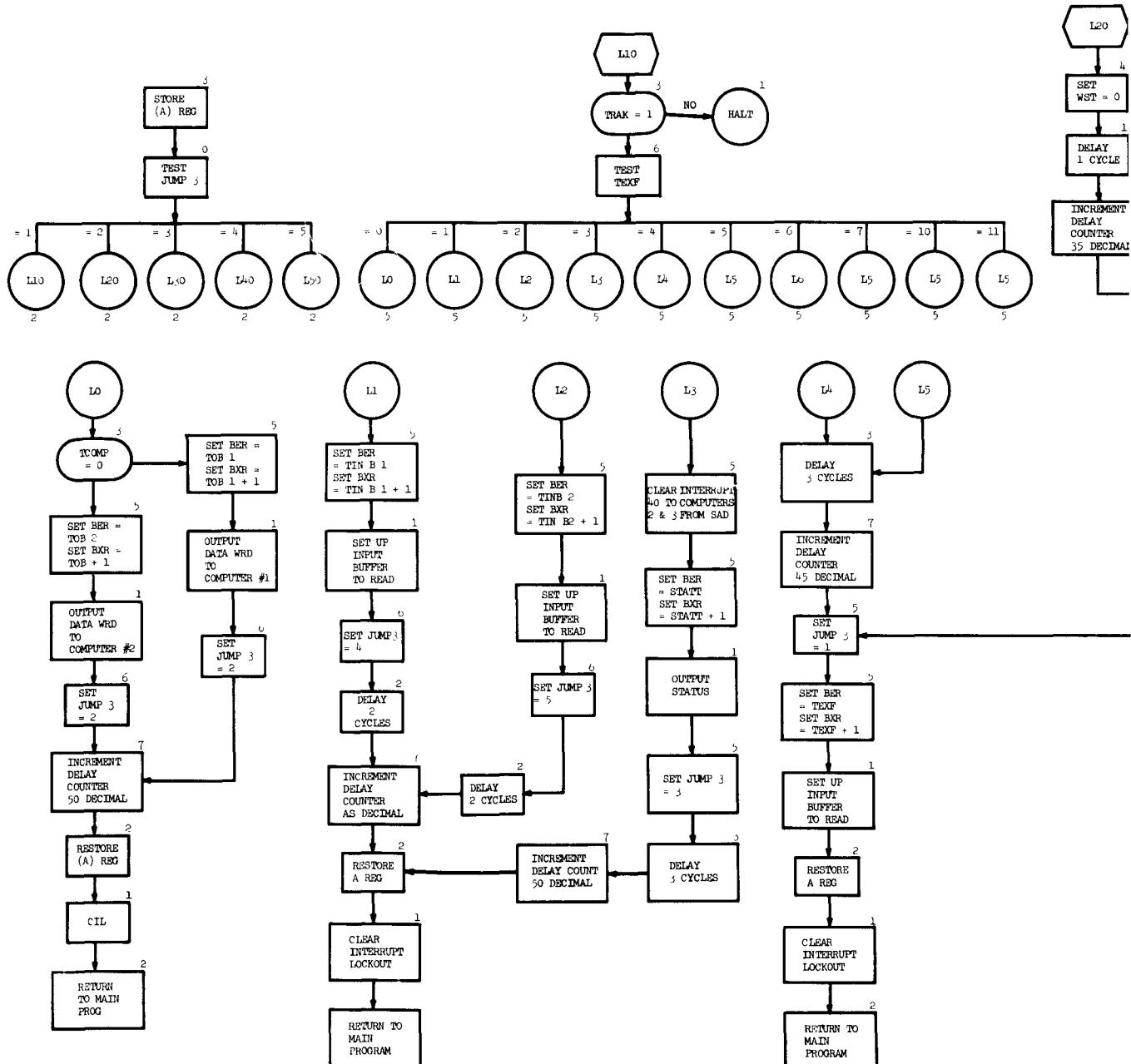
TM-1003/010/0

2



1

26 March 1963

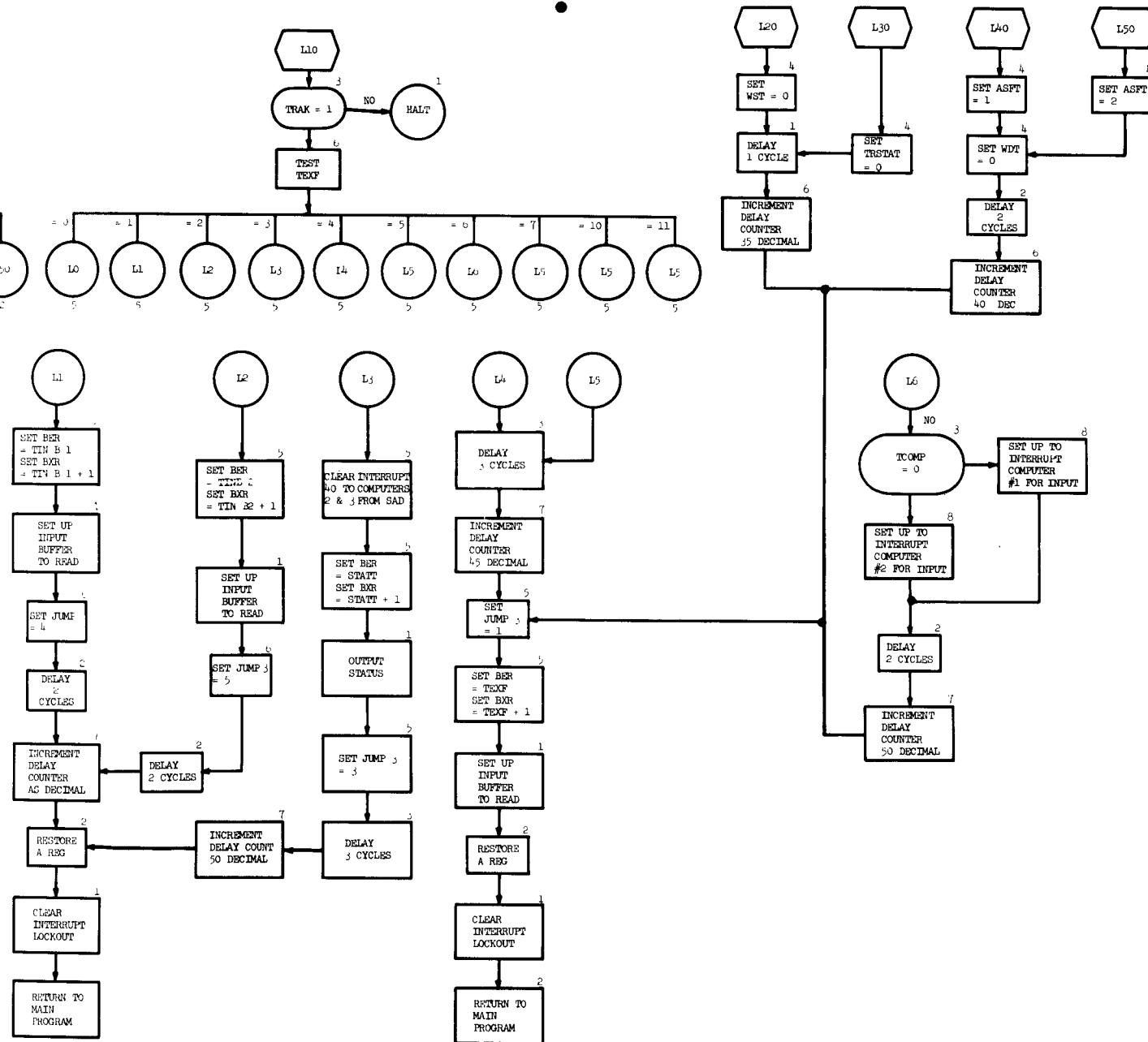


26 March 1963

-14-

TM-1003/010/0

2



26 March 1963

-15-

TM-1003/010/00

APPENDIX B

0000	0000	CON	0	
0000	0060	SID0	0	
0001	7101	JFI	1	SET I AND 7 BANKS TO ZERO
0002	0712			START
0003	0000	ASFT		
0004	0000	ASF8		AUXIL SEND FLAG TS
0005	0000	TME		AUXIL SEND FLAG BB
0006	0000	TCOMP		TS COMPUTER
0007	0000	BCOMP		BB COMPUTER
0010	0000	INT10		
0011	7101	JFI	1	
0012	1613	UPBUF		
0013	0000	LRTS		LAST REC TS
0014	0000	LBBB		LAST REC BB
0015	0000	SFT		SEND FLAG TS
0016	0000	SFB		SEND FLAG BB
0017	0000	AREG		A REGISTER
0020	0000	INT20	0	
0021	4017	STD	AREG	
0022	7101	JUMP3	JFI	1
0023	0412			L10
0024	0616			L20
0025	0624			L30
0026	0632			L40
0027	0643			L50
0030	0000	INT30	0	
0031	4017	STD	AREG	
0032	7101	JFI	1	
0033	0100	R30		
0040	0000	CON	40	
0041	4017	STD	AREG	
0042	7101	JFI	1	
0043	0110	R40		
0050	0000	CON	50	
0050	0000	TRSTAT		STATUS ASKED TS
0051	0000	WST		WORD PU
0052	0000	WPT		WORD SENT
0053	0000	TSRDY		RDY TO SEND FLAG
0054	0000	TSR		TS REC FLAG
0055	0000	TSKIP		TS SKIP REC FLAG
0056	0000	BBSTAT		
0057	0000	WSB		
0060	0000	WPB		
0061	0000	BSR		
0062	0000	BSKIP		
0063	0000	BURDY		
0064	0000	STATW		BB STATUS WORD
0065	0000	STATT		TS
0066	0000	TIMB		
0067	0000	JUNK		
0070	0000	BIRD		
0071	0000	TRAK		
0100	0100	PRG	100	
0100	7500	R30	EXC	4702
0101	4702			
0102	7101	JUMP1	JFI	1
0103	0143			X10
0104	0390			X20
0105	0396			X30

26 March 1963

-16-

TM-1003/010/00

0106	0364		x40	
0107	0375		x50	
0110	7500	440	EXC	30
0111	0030			
0112	2070		LDD	BIRD
0113	6104		NZF	4
0114	7700		MLT	
0115	7101		JFI	1
0116	0712			BB NOT IN TIME
0117	7500		EXC	4701
0120	4701			
0121	7315		OUT	15
0122	0143			R *4
0123	2200		LDC	7101
0124	7101			
0125	4100		STM	JUMP1
0126	0102			
0127	2200		LDC	40D
0130	0050			
0131	5067		HAD	JUNK
0132	2010		LDD	INT10
0133	2017		LDD	AREQ
0134	0120		CIL	
0135	7040		JPI	INT40
0136	0137			R
0137	4012	R		4012
0140	0700			EXF
0141	0701			EXF *1
0142	0000			0
0143	0022	x10	HEM	ANAL EXF 30 INT
0144	2100		SIC2	
0145	0700		LDM	EXF
0146	0020		SICO	
0147	0277		LPA	77
0150	3200		ADC	7101
0151	7101			
0152	4201		STF	1
0153	0000			0
0154	0166		X0	3500
0155	0230		X1	01
0156	0246		X2	02
0157	0271		X3	03
0160	0312		X4	04
0161	0317		X5	05
0162	0324		X6	06
0163	0317		X7	07
0164	0317		X8	10
0165	0317		X9	11
0166	2007	x0	LDD	WCOMP
0167	6033		ZJF	X0,1
0170	7500		EXC	4701
0171	4701			COMP 2
0172	7307		OUT	7
0173	0224			X0,5 *4
0174	2200		LDC	7102
0175	7102			
0176	4100		STM	JUMP1
0177	0102			
0200	6314		NJF	X0,4

26 March 1963

-17-

TM-1003/010/00

0201	0220				
0202	7500	x0.1	EXC	4701	COMP 1
0203	4701				
0204	7307		OUT	7	
0205	0240			x0.6	*4
0206	2200		LDC	7102	
0207	7102				
0210	4100		STW	JUMP1	
0211	0102				
0212	6302		NJF	x0.4	
0213	0224			x0.6	
0214	2200	x0.4	LDC	550	NO CYCLES#5500
0215	0067				
0216	7101		JFI	1	
0217	0344			x8	
0220	4002	x0.5		4002	
0221	0704			082	
0222	0705			082	*1
0223	0000			0	
0224	4002	x0.6		4002	
0225	0703			091	
0226	0704			081	*1
0227	0000			0	
0230	7500	x1	EXC	4701	
0231	4701				
0232	7307		OUT	7	
0233	0246			x1.5	*4
0234	2200		LDC	7104	
0235	7104				
0236	4100		STW	JUMP1	
0237	0102				
0240	6324		NJF	x2.6	
0241	0242			x1.5	
0242	4012	x1.5		4012	
0243	0701			INR1	
0244	0702			INR1	*1
0245	0000			0	
0246	7500	x2	EXC	4701	
0247	4701				
0250	7307		OUT	7	
0251	0264			x2.5	*4
0252	2200		LDC	7105	
0253	7105				
0254	4100		STW	JUMP1	
0255	0102				
0256	6306		NJF	x2.6	
0257	0260			x2.5	
0260	4012	x2.5		4012	
0261	0702			INR2	
0262	0703			INR2	*1
0263	0000			0	
0264	2200	x2.6	LDC	550	NO CYCLES 71#2
0265	0067				
0266	4020		STW	INT20	
0267	7101		JFI	1	
0270	0344			x8	
0271	7500	x3	EXC	4701	
0272	4701				
0273	7312		OUT	12	

26 March 1963

-18-

TM-1003/010/00

0274	0312		X3.5	+4
0275	2200	LDC	7103	
0276	7103			
0277	4100	STM	JUMP1	
0300	0102			
0301	2200	LDC	551	
0302	0067			NO CYC. 03
0303	7101	UFI	1	
0304	0344		X8	
0305	0306		X3.5	
0306	4002	x3.5	4002	
0307	0064		STATW	
0310	0065		STATW	+1
0311	0000		0	
0312	2200	x4	LDC	400
0313	0050			NO CYC 04
0314	4100	STM	INT10	
0315	0010			
0316	6226	PJF	X8	
0317	2200	x5	LDC	400
0320	0050			DISREGARD 45
0321	4100	STM	INT10	
0322	0010			
0323	6221	PJF	X8	
0324	2007	x6	LDD	HCOMP
0325	6006		ZJF	X6,0
0326	2061		LDD	BRR
0327	0201		LPA	1
0330	0602		ADA	2
0331	4061		STD	BRR
0332	6206	PJF	X6,1	
0333	2061	x6,0	LDD	BRR
0334	0202		LPA	2
0335	0601		ADA	1
0336	4061		STD	BRR
0337	6201	PJF	X6,1	
0340	2200	x6,1	LDC	500
0341	0062			NO CYC 06
0342	4100	STM	INT10	
0343	0010			
0344	5067	x8	RAD	JUNK
0345	2017	LDD	AREG	
0346	0120	CIL		
0347	7030	JPI	INT30	
0350	0400	x20	LDA	0
0351	4057		STD	WSB
0352	2200		LDC	30D
0353	0036			NO CYC AFTER 5500
0354	4010		STD	INT10
0355	6231		PJF	X55
0356	0400	x30	LDA	0
0357	4056		STD	WSSTAT
0360	2200		LDC	30D
0361	0036			NO CYC AFTER 5503
0362	4010		STD	INT10
0363	6223		PJF	X95
0364	0400	x40	LDA	0
0365	4060		STD	WPR
0366	0401		LDA	1
0367	4004		STD	ASFB

26 March 1963

-19-

TM-1003/010/00

0370	2200		LDC	35D	
0371	0043		STM	INT10	
0372	4100				
0373	0010				
0374	6212				
0375	0400	x50	PJF	X55	
0376	4060		LDN	0	
0377	0402		STD	WPB	
0400	4004		LDN	2	
0401	2200		STD	ASFB	
0402	0043		LDC	35D	NO CYC AFTER 5501
0403	4100		STM	INT10	
0404	0010				
0405	6201		PJF	X55	
0406	5067	x55	HAD	JUNK	
0407	2017		LDN	AREG	
0410	0120		CIL		
0411	7030		JPI	INT30	
0412	2071	L10	LDN	TRAK	
0413	6104		NZF	4	
0414	7700		MLT		
0415	7101		JFI	1	
0416	0712		START		
0417	2100		LDN	TEXF	
0420	0705				
0421	0277		LPA	77	
0422	3200		ADC	7101	
0423	7101		STF	1	
0424	4201			0	
0425	0000				5500
0426	0440		LD		
0427	0500		L1		01
0430	0515		L2		02
0431	0540		L3		03
0432	0562		L4		04
0433	0566		L5		05
0434	0572		L6		06
0435	0566		L5		07
0436	0566		L5		10
0437	0566		L5		11
0440	2006	L0	LDN	TCOMP	
0441	6016		ZJF	L0,1	
0442	2200		LDC	T0B2	COMP2
0443	0711				
0444	0105	L00,1	ATE	L00,1	
0445	0444				
0446	0601		ADN	1	
0447	0106		ATX	L00,1	♦5
0450	0447				
0451	7300		I80	L00,1	♦5
0452	0451				
0453	2200		LDC	7102	
0454	7102				
0455	4022		STD	JUMPS	
0456	6316		NJF	L0,4	
0457	2200	L0,1	LDC	T0B1	
0460	0710				
0461	0105	L00,2	ATE	L00,2	
0462	0461				
0463	0601		ADN	1	

26 March 1963

-20-

TM-1003/010/00

0464	0106		ATX	L00,2	+	3
0465	0464					
0466	7300		I80	L00,2	+	2
0467	0466					
0470	2200		LDC	7102		
0471	7102					
0472	4022		STD	JUMPS		
0473	6301		NJF	L0,4		
0474	2200	L0,4	LDC	50D		
0475	0062					
0476	7101		JFI	1		
0477	0612			L8		
0500	2200	L1	LDC	TINR1		
0501	0706					
0502	0105	L11,1	ATE	L11,1		
0503	0502					
0504	0601		ADA	1		
0505	0106		ATX	L11,1	+	3
0506	0505					
0507	7200		I81	L11,1	+	2
0510	0507					
0511	2200		LDC	7104		
0512	7104					
0513	4022		STD	JUMPS		
0514	6316		NJF	L2,5		
0515	2200	L2	LDC	TINR2		
0516	0707					
0517	0105	L22,1	ATE	L22,1		
0520	0517					
0521	0401		ADA	1		
0522	0106		ATX	L22,1	+	3
0523	0522					
0524	7200		I81	L22,1	+	2
0525	0524					
0526	2200		LDC	7105		
0527	7105					
0530	4022		STD	JUMPS		
0531	6301		NJF	L2,5		
0532	2200	L2,6	LDC	50D		NO CYC 01-2
0533	0062					
0534	0277		LPN	77		
0535	0277		LPA	/7		
0536	7101		JFI	1		
0537	0612			L8		
0540	7500	L3	EXC	30		
0541	0030					
0542	2200		LDC	STATT		
0543	0065					
0544	0105	L33,1	ATE	L33,1		
0545	0544					
0546	0601		ADA	1		
0547	0106		ATX	L33,1	+	3
0550	0547					
0551	7300		I80	L33,1	+	2
0552	0551					
0553	2200		LDC	7103		
0554	7103					
0555	4022		STD	JUMPS		
0556	2200		LDC	50D		NO CYC 5503
0557	0062					

26 March 1963

-21-

TM-1003/010/00

0560	7101	JFI	1	
0561	0612		L8	
0562	2200	L4	LDC	45D
0563	0055			NO CYCLES 5504
0564	7101	JFI	1	
0565	0654		L55	
0566	2200	L5	LDC	45D
0567	0055			
0570	7101	JFI	1	
0571	0654		L55	
0572	2006	L6	LDD	TCO4P
0573	6006		ZJF	L6,0
0574	2054		LDD	TSR
0575	0201		LPN	1
0576	0602		ADN	2
0577	4054		STD	TSR
0600	6206		PJF	L6,1
0601	2054	L6,0	LDD	TSR
0602	0202		LPN	2
0603	0601		ADN	1
0604	4054		STD	TSR
0605	6201		PJF	L6,1
0606	2200	L6,1	LDC	50D
0607	0062			
0610	7101	JFI	1	
0611	0654		L55	
0612	5067	L8	NAD	JUNK
0613	2017		LDD	AREQ
0614	0120		CIL	
0615	7020		JPI	INT20
0616	0400	L20	LDN	0
0617	4051		STD	HST
0620	2200		LDC	35D
0621	0043			NO CYCLE AFTER 5500
0622	0277		LPN	77
0623	6231		PJF	L55
0624	0400	L30	LDN	0
0625	4050		STD	TRSTAT
0626	2200		LDC	35D
0627	0043			NO CYCLE AFTER 5503
0630	0277		LPN	77
0631	6223		PJF	L55
0632	0400	L40	LDN	0
0633	4092		STD	HPT
0634	0401		LDN	1
0635	4003		STD	ASFT
0636	2200		LDC	40D
0637	0080			NO CYCLE AFTER 5501
0640	0277		LPN	77
0641	0277		LPN	77
0642	6212		PJF	L55
0643	0400	L50	LDN	0
0644	4092		STD	HPT
0645	0402		LDN	2
0646	4003		STD	ASFT
0647	2200		LDC	40D
0650	0050			NO CYCLE AFTER 5502
0651	0277		LPN	77
0652	0277		LPN	77
0653	6201		PJF	L55

26 March 1963

-22-

TM-1003/010/00

0654	5067	L55	MAD	JUNK
0655	2200	LDC	7101	
0656	7101			
0657	4022	STD	JUMPS	
0660	2200	LDC	TEXF	
0661	0705			
0662	0105	L55,5	ATE	L55,5
0663	0662			
0664	0601	ADA	1	
0665	0106	ATX	L55,5	++
0666	0665			
0667	7200	I8I	L55,5	++
0670	0667			
0671	2017	LDD	AREQ	
0672	0120	CIL		
0673	7020	JPI	INT20	
0674	0404	?	404	1 RDY TO REC
0675	1004		1004	2
0676	0400		400	U NOT RDY REC
0677	1000		1000	2
0700	0000	EXF		
0701	0000	INR1		
0702	0000	INR2		
0703	0000	O81		
0704	0000	O82		
0705	0000	TEXF		
0706	0000	TINB1		
0707	0000	TINB2		
0710	0000	TOR1		
0711	0000	TOR2		
0712	0400	START	LDN	0
0713	4003			INITIALIZE
0714	4004	STD	ASFT	
0715	4005	STD	ASFB	
0716	4066	STD	TIME	
0717	4055	STD	TIWA	
0720	4062	STD	TSKIP	
0721	0140		SSU0	
0722	0401	LDN	2	
0723	4006	STD	TCOMP	
0724	4007	STD	BCOMP	
0725	4013	STD	LRTS	
0726	4014	STD	LRBA	
0727	0403	LDN	3	
0730	4061	STD	B8R	
0731	4054	STD	T8R	
0732	7500	EXC	4702	
0733	4702			
0734	0120	CIL		
0735	2200	LDC	7101	
0736	7101			
0737	4022	STD	JUMPS	
0740	0400	LDA	0	IDLE
0741	6601	PJ8	1	
		HEM		
0742	2005	75	LDD	TIME
0743	6003		ZJP	3
0744	7101		JFI	1
0745	1045		A0,8	
0746	0401	LDN	1	187 TIME

26 March 1963

-23-

TM-1003/010/00

0747	4005		STD	TIME	
0750	2003		LDD	ASFT	
0751	4016		STD	SFT	
0752	0701		SBN	1	
0753	6322		NJF	A0,2	
0754	6111		NZF	A0,1	
0755	2100		LDM	TIN#1	COMP 1
0756	0706				
0757	0022		SIC2		
0760	4100		STM	0B1	
0761	0703				
0762	0020		SIC0		
0763	7101		JFI	1	
0764	1003			A0,3	
0765	2100	A0,1	LDM	TIN#2	COMP 2
0766	0707				
0767	0022		SIC2		
0770	4100		STM	0B2	
0771	0704				
0772	0020		SIC0		
0773	7101		JFI	1	
0774	1003			A0,3	
0775	2100	A0,2	LDM	INT10	NEITHER 12 DELAY
0776	0010				
0777	4100		STM	INT10	
1000	0010				
1001	4010		STD	INT10	
1002	4010		STD	INT10	
1003	2004	A0,3	LDD	ASFT	
1004	4015		STD	SFT	
1005	0701		SBN	1	
1006	6322		NJF	A0,6	
1007	6111		NZF	A0,5	
1010	0022		SIC2		
1011	2100		LDM	INB1	COMP 1
1012	0701				
1013	0020		SIC0		
1014	4100		STM	T0B1	
1015	0710				
1016	7101		JFI	1	
1017	1037			A0,7	
1020	0022	A0,5	SIC2		COMP 2
1021	2100		LDM	INB2	
1022	0702				
1023	0020		SIC0		
1024	4100		STM	T0B2	
1025	0711				
1026	7101		JFI	1	
1027	1037			A0,7	
1030	2100	A0,6	LDM	INT10	NEITHER 12 DELAY
1031	0010		STM	INT10	
1032	4100				
1033	0010				
1034	2010		LDD	INT10	
1035	4004		STD	ASFT	
1036	4003		STD	ASFT	
1037	0400	A0,7	LDM	0	
1040	4010		STD	INT10	
1041	2013		LDD	LRTS	COMR=OPPOS LRTS
1042	0301		SBN	1	

26 March 1963

-24-

TM-1003/010/00

1043	4006		STD	TCOMP	
1044	6215		PJF	A1	
1045	0400	A0,8	LDN	0	
1046	4005		STD	TIME	
1047	0503		LCA	3	
1050	4067		STD	JUNK	
1051	2100	A0,9	LDN	INT10	
1052	0010				
1053	4100		STM	INT10	
1054	0010				
1055	0501		LCA	1	
1056	5467		ACD	JUNK	
1057	6706		NJB	A0,9	
1060	2010		LOD	INT10	
1061	0401	A1	LDN	1	
1062	4050		STD	THSTAT	
1063	4051		STD	WST	
1064	4052		STD	WPT	
1065	4071		STD	TRAK	
1066	2006	A10	LOD	TCOMP	
1067	6154		NZF	A25	
1070	2054		LOD	TSR	IF COMP 2 COMP 1
1071	0201		LPN	1	
1072	6034		ZJF	A11	
1073	2055		LOD	TSKIP	
1074	6134		NZF	A11	*2
1075	2100		LDN	INT10	DELAY 7
1076	0010				
1077	4100		STM	INT10	
1100	0010				
1101	2100		LDN	T	
1102	0674				
1103	4065		STD	STATT	
1104	2015		LOD	SFT	
1105	0201		LPN	1	
1106	6011		ZJF	A20	
1107	0400	A19	LDN	0	
1110	4019		STD	SFT	
1111	2005		LOD	STATT	
1112	0601		ADN	1	
1113	4005		STD	STATT	
1114	0401		LDN	1	
1115	4053	419,9	STD	TSROY	
1116	6293		PJF	A39,9	*1
1117	0400	A20	LDN	0	
1120	4100		STM	INT10	DELAY 11
1121	0010				
1122	4100		STM	INT10	
1123	0010				
1124	0400		LDN	0	
1125	6610		PJF	A19,9	
1126	2100	A11	LDN	INT10	
1127	0010				
1130	0400		LDN	0	
1131	4055		STD	TSKIP	
1132	2100		LDN	T	*2
1133	0676				
1134	4100		STM	STATT	
1135	0065				

26 March 1963

-25-

TM-1003/010/00

1136	2015		LDD	SFT	
1137	0201		LPA	1	
1140	6531		NZB	A19	
1141	7101		JFI	1	
1142	1313			A99	
1143	2054	A25	LDD	TSR	
1144	0202		LPN	2	
1145	6034		ZJF	A31	
1146	2055		LDD	TSKIP	
1147	6134		NZF	A31	+2
1150	2100		LDM	INT10	DELAY 7
1151	0010		STM	INT10	
1152	4100				
1153	0010		LDM	T	+1
1154	2100				
1155	0675		STD	STATT	
1156	4065		LDD	SFT	
1157	2015		LPN	2	
1160	0202		ZJF	A40	
1161	6011		LDM	0	
1162	0400	A39	STD	SFT	
1163	4015		LDD	STATT	
1164	2065		ADA	1	
1165	0601		STD	STATT	
1166	4065		LDM	1	
1167	0401		STD	TSRDY	
1170	4053	A39,9	PJF	A50	
1171	6225		LDM	0	DELAY 11
1172	0400	A40	STM	INT10	
1173	4100				
1174	0010		STD	INT10	
1175	4100		LDM	0	
1176	0010		PJF	A39,9	
1177	0400		LDM	INT10	
1200	6610				
1201	2100	A31	LDM	0	
1202	0010		LDN	0	
1203	0400		STD	TSKIP	
1204	4055		LDM	T	+3
1205	2100		STD	STATT	
1206	0677		STM	SFT	
1207	4100		LDD	STATT	
1210	0065		LPN	2	
1211	2015		NZB	A39	
1212	0202		JFI	1	
1213	6531			A99	
1214	7101		EXC	10	INTERRUPT TS
1215	1313				
1216	7500	A50	CIL		
1217	0010		LCC	2900	
1220	0120				
1221	2600		STD	JUNK	
1222	0442		LDN	5	
1223	4067		NAD	JUNK	
1224	0405		NJB	2	
1225	5067		LDN	0	
1226	6702		STD	TRAK	
1227	0400		LCN	50D	
1230	4071				
1231	0562				

26 March 1963

-26-

TM-1003/010/00

1232	5067		HAD	JUNK	
1233	6204		PJF	4	
1234	0405		LDR	5	
1235	5067		HAD	JUNK	
1236	6702		NJH	2	
1237	2050		LOD	TRSTAT	
1240	6130		NZF	A90	
1241	2053		LOD	TSRDY	
1242	6016		ZJF	A85	
1243	2051		LOD	WST	WAS ABLE SEND
1244	6127		NZF	A91	
1245	2052	A80	LOD	WPT	
1246	6114		NZF	A87	
1247	0401		LOD	1	WORD REC
1250	4055		STD	TSKIP	
1251	2006		LOD	TCOMP	
1252	4013		STD	LRTS	
1253	2006	A80	LOD	TCOMP	
1254	0301		SCN	1	
1255	4006		STD	TCOMP	
1256	7101		JFI	1	
1257	1323			BB	
1260	2051	A85	LOD	WST	DELAY 3
1261	6614		PJF	A60	
1262	2100	A87	LOD	INT10	DELAY 9
1263	0010				
1264	4100		STM	INT10	
1265	0010				
1266	7101		JFI	1	
1267	1293			A80	
1270	7701	A90	SLS1		
1271	7101		JFI	1	
1272	1274			A91	+1
1273	7702	A91	SLS2		
1274	7500		EXC	30	
1275	0030				
1276	0120		GIL		
1277	0104		CBC		
1300	2200		LDC	TEXF	
1301	0705				
1302	0105	A91,1	ATE	A91,1	
1303	1302				
1304	0601		ADA	1	
1305	0106	A91,2	ATX	A91,2	
1306	1305				
1307	7200	A91,3	IBI	A91,3	
1310	1307				
1311	7101		JFI	1	
1312	1253			A80	
1313	2600	A99	LCC	4250	
1314	0651				
1315	4067		STD	JUNK	
1316	0405		LDR	5	
1317	5067		HAD	JUNK	
1320	6702		NJH	2	
1321	7101		JFI	1	
1322	1293			A80	
1323	2066	88	REM		BIRD CYCLE
			LOD	TIME	

26 March 1963

-27-

TM-1003/010/00

1324	6106		NZF	B81	
1325	0401		LDA	1	
1326	4100		STM	TIMB	
1327	0066				
1330	7101		JFI	1	
1331	1340			B4B	
1332	0400	B81	LDA		
1333	4006		STD	TIMB	
1334	0400		LDA		DELAY
1335	4100		STD	INT10	
1336	0010				
1337	6204		PJF	B8B	+3
1340	2014	B82	LDD	LRAA	
1341	0301		SCA	1	
1342	4007		STD	BCO4P	
1343	0401		LDA	1	
1344	4056		STD	B8STAT	
1345	4057		STD	WS8	
1346	4060		STD	WP8	
1347	4070		STD	Y1P0	
1350	2007		LDD	BCC4P	
1351	6163		NZF	B25	IF COMP 2
1352	2061		LDD	B8R	
1353	0201		LPN	1	
1354	6042		ZJF	B11	
1355	2062		LDD	B8K1P	
1356	6142		NZF	B11	+2
1357	2100		LDM	INT10	DELAY 7
1360	0010				
1361	4100		STM	INT10	
1362	0010				
1363	2100		LDM	T	
1364	0674				
1365	0042		SDC2		
1366	4064		STD	STATB	
1367	0040		SDC0		
1370	2016		LDD	SFB	
1371	0201		LPN	1	
1372	6014		ZJF	B20	
1373	0400	B19	LDA	0	
1374	4016		STD	SFB	
1375	0042		SDC2		
1376	2064		LDD	STATB	
1377	0601		ADA	1	
1400	4064		STD	STATB	
1401	0040		SDC0		
1402	0401		LDA	1	
1403	4063	B19,9	STD	B8RDY	
1404	7101		JFI	1	
1405	1515			B50	
1406	0400	B20	LDA	0	DELAY 13
1407	4100		STM	INT10	
1410	0010				
1411	4100		STM	INT10	
1412	0010				
1413	4010		STD	INT10	
1414	0400		LDA	0	
1415	6612		PJB	B19,9	
1416	2100	B11	LDM	INT10	
1417	0010				

26 March 1963

-28-

TM-1003/010/00

1420	0400		LDN	0	
1421	4062		STD	BSKIP	
1422	2100		LDM	T	+2
1423	0676				
1424	0042		SDC2		
1425	4064		STD	STATB	
1426	0040		SDC2		
1427	2016		LDD	SFB	
1430	0201		LPA	1	
1431	6536		NZB	019	
1432	7101		JFI	1	
1433	1602			099	
1434	2061	W25	LDD	00R	
1435	0202		LPA	2	
1436	6040		ZJF	031	
1437	2062		LDD	BSKIP	
1440	6140		NZF	031	+2
1441	2100		LDM	INT10	DELAY 7
1442	0010				
1443	4100		STM	INT10	
1444	0010				
1445	2100		LDM	T	+1
1446	0675				
1447	0042		SDC2		
1450	4064		STD	STATB	
1451	0040		SDC2		
1452	2016		LDD	SFB	
1453	0202		LPA	2	
1454	6013		ZJF	040	
1455	0400	W39	LDN	0	
1456	4016		STD	SFB	
1457	0042		SDC2		
1460	2064		LDD	STATB	
1461	0601		ADN	1	
1462	4064		STD	STATB	
1463	0040		SDC2		
1464	0401		LDN	1	
1465	4063	W39,9	STD	BSRDY	
1466	6227		PJF	050	
1467	0400	W40	LDN	0	
1470	4100		STM	INT10	DELAY 13
1471	0010				
1472	4100		STM	INT10	
1473	0010				
1474	4010		STD	INT10	
1475	6610		PJF	039,9	
1476	2100	W31	LDM	INT10	
1477	0010				
1500	0400		LDN	0	
1501	4062		STD	BSKIP	
1502	2100		LDM	T	+3
1503	0677				
1504	0022		SIC2		
1505	4100		STM	STATB	
1506	0064				
1507	0020		SIC2		
1510	2016		LDD	SFB	
1511	0202		LPA	2	
1512	6535		NZB	039	
1513	7101		JFI	1	

26 March 1963

-29-

TM-1003/010/00

1514	1602					
1515	7500	950	EXC	20	899	INTERRUPT 4B
1516	0020					
1517	0120		CIL			
1520	2600		LCC	3150		
1521	0473					
1522	4067		STD	JUNK		
1523	0405		LDA	5		
1524	5067		HAD	JUNK		
1525	6702		NJB	2		
1526	0400		LDA	0		
1527	4070		STD	8180		
1530	0562		LDA	50D		
1531	5067		HAD	JUNK		
1532	6204		WIF	4		
1533	0405		LDA	5		
1534	5067		HAD	JUNK		
1535	6702		NJB	2		
1536	2056		LOD	88STAT		
1537	6130		NZF	890		
1540	2063		LOD	88RDY		
1541	6016		ZIF	885		
1542	2057		LOD	WSB		WAS ABLE SENJ
1543	6127		NZF	891		
1544	2060	860	LOD	WPS		
1545	6114		NZF	887		
1546	0401		LDA	1		WORD REC
1547	4062		STD	85KIP		
1550	2007		LOD	8COMP		
1551	4014		STD	LRBS		
1552	2007	880	LOD	8COMP		
1553	0301		SCA	1		
1554	4007		STD	8COMP		
1555	7101		JFI	1		
1556	0742			TS		
1557	2057	885	LOD	WSB		
1560	6614		PJE	880		DELAY 3
1561	2100	887	LDM	INT10		DELAY 9
1562	0010		STM	INT10		
1563	4100					
1564	0010		JFI	1		
1565	7101			880		
1566	1552					
1567	7701	890	SLS1			
1570	7101		JFI	1		
1571	1573			891	+1	
1572	7702	891	SLS2			
1573	7500		EXC	30		
1574	0030					
1575	7500		EXC	4702		
1576	6702		CIL			
1577	0120		JFI	1		
1600	7101			880		
1601	1552					
1602	2600	999	LCC	463D		
1603	0717					
1604	4067		STD	JUNK		
1605	0405		LDA	5		
1606	5067		HAD	JUNK		
1607	4702		NJB	2		

26 March 1963

-30-
(last page)

TM-1003/010/00

1610	0400	LDA	0
1611	7101	JFI	1
1612	1552		BB0
1613	2200	UPRUF	LDC
1614	0705		TEXP
1615	0105	A00,1	ATE
1616	1615		A00,1
1617	0601		ADN
1620	0106	A00,2	ATX
1621	1620		A00,2
1622	7200	A00,3	ISI
1623	1622		A00,3
1624	7101	JFI	1
1625	0742		TS
	0000	END	

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UNCLASSIFIED

System Development Corporation,
Santa Monica, California

MILESTONE 11 160A COMPUTER PROGRAM

DESCRIPTION.

Scientific rept., TM-1003/010/00,
by V. J. Gergen. 26 March 1963, 30p.
(Contract AF 19(628)-1648, Space Systems
Division Program, for Space Systems
Division, AFSC)

Unclassified report

DESCRIPTORS: Programming (Computers).
Satellite Networks.

UNCLASSIFIED

Reports that the CCC Simulator provides
a simulated intercommunication link
between the Bird Buffer (BB) computer
and the Tracking Station (TS) computer
that is normally performed by the
Computer Communication Converter (CCC)
and associated equipment.

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